SYSTEM FOR COUPLING PROGRAMMABLE LOGIC DEVICE TO EXTERNAL CIRCUITRY WHICH SELECTS A LOGIC STANDARD AND USES BUFFERS TO MODIFY OUTPUT AND INPUT SIGNALS ACCORDINGLY

BACKGROUND OF THE INVENTION

This invention relates to programmable logic devices ("PLDs"), and more particularly to a new architecture for the input/output (I/O) circuitry which couples the PLDs to external circuitry.

Programmable logic devices are integrated circuits which are able to implement combinational and/or sequential digital functions which may be defined by a designer and programmed into the device. Thus, PLDs may be configured by a user to implement any Boolean expression or registered function with built-in logic structures. Once a PLD is configured, the user must connect the PLD to external circuitry which provides input signals to, and receives output signals from, the PLD.

One deficiency of conventional PLDs and their I/O circuitry is that each PLD must be configured to operate with specific external circuitry. For example, if a user utilizes Transistor-to-Transistor Logic (TTL) or CMOS external circuitry, the PLD must be configured to provide the appropriate drive signals. However, the selection of open drain logic may require different drive parameters and thus, a different PLD, even though the basic PLD is substantially the same. This deficiency is even more apparent in view of the programmable nature of PLDs and the flexibility provided to the end users.

Further, the nature of PLDs, as semiconductor devices, is that they are susceptible to a wide range of potential hazards, such as electrostatic discharge (ESD). To avoid these potential problems, care must be taken in connecting the PLD pins to external circuitry. Any pins which are used as input pins should preferably be driven by an active source (including bi-directional pins during input operations). Additionally, unused pins are typically tied to ground to avoid the potential of additional DC current and noise being introduced into the circuits.

Output loading of the PLD I/O pins is typically resistive and/or capacitive. Resistive loading exists where the device output sinks or sources a current during steady-state operation (e.g., TTL inputs, terminated buses, and discrete bipolar transistors). Capacitive loading typically occurs from packaging and printed circuit board traces. Further, an important design consideration of the interface between the PLD and external circuitry is that the target device can supply both the current and speed necessary for the given loads.

Various attempts have also been made at providing interface circuitry that operates at lower power levels, for example, the Gunning Transistor Logic (GTL) interface described in Gunning U.S. Pat. No. 5,023,488. GTL interface drivers typically operate with a voltage swing on the order of about 0.8 volts to 1.2 volts, which are intended to drive a CMOS binary communications bus. Another interface, High-Speed Transistor Logic (HSTL) typically operates with a voltage swing of about a predetermined voltage plus 0.050 volts to the predetermined voltage minus 0.050 volts and at relatively higher switching frequencies than GTL (for terminated HSTL, the predetermined voltage is the termination voltage, while non-terminated HSTL uses a reference voltage).

One deficiency of Gunning and other known driver circuitry is the limited scope with which the circuitry may be used. A PLD having GTL drivers must interface with a GTL bus. A PLD having TTL drivers must interface with a TTL bus or discrete TTL components. A PLD having HSTL drivers must interface with a HSTL bus or discrete HSTL components.

In view of the foregoing, it would be desirable to be able to provide an I/O architecture which provides the capability to drive multiple logic standards.

It would also be desirable to be able to provide an I/O architecture having the capability to selectively drive any one of multiple logic standards.

It would further be desirable to be able to provide an I/O architecture which may be programmed by a user to select any one of several logic standards, such that a single PLD may be used with external circuitry that operates at different logic levels.

SUMMARY OF THE INVENTION

It is an object of this invention to provide an I/O architecture which provides the capability to drive multiple logic standards.

It is a further object of this invention to provide an I/O architecture having the capability to selectively drive any one of multiple logic standards.

It is a further object of this invention to provide an I/O architecture which may be programmed by a user to select any one of several logic standards, such that a single PLD may be used with external circuitry that operates at different logic levels.

These and other objects are accomplished in accordance with the principles of the present invention by providing an I/O architecture which includes programmable I/O buffers that interface with various different logic standards. In a preferred embodiment of the present invention, programmable I/O devices are provided which interface with TTL, CMOS, open drain, GTL and HSTL (both terminated and non-terminated) logic standards. Those skilled in the art will understand that other logic standards, both those presently available and others still to be developed, may be incorporated into I/O circuits such as those described herein without departing from the scope of the present invention.

The preferred embodiment of the present invention provides a programmable logic circuit having four states (i.e., two bits) which are correspond to voltage levels representative of various logic standards. By adding an additional bit to the logic circuit and additional driving circuitry, additional logic standards may be supported.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects and advantages of the invention will be apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings, in which like reference numerals refer to like parts throughout, and in which:

FIG. 1 is a schematic block diagram of an illustrative embodiment of an input/output circuit incorporating principles of the present invention;

FIG. 2 is a schematic diagram of a programmable output buffer of the input/output circuit of FIG. 1, constructed in accordance with the principles of the present invention;

FIG. 3 is a schematic diagram of one embodiment of a programmable input buffer of the input/output circuit of FIG. 1, constructed in accordance with the principles of the present invention;

FIG. 4 is a schematic diagram of an alternate embodiment of a programmable input buffer of the input/output circuit of FIG. 1, constructed in accordance with the principles of the present invention;

FIG. 5 is a schematic diagram of another alternate embodiment of a programmable input buffer of the input/output circuit of FIG. 1, constructed in accordance with the principles of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 shows a schematic block diagram of a programmable input/output (I/O) circuit **100** which incorporates principles of the present invention. I/O circuit **100** includes output driver **102**, input driver **104**, I/O pad **106**, and programmable elements **108** and **110**. Output driver **102**, which has an input terminal to receive output signals from a programmable logic device (PLD) (not shown), provides an output signal (OUT) to I/O pad **106** at an appropriate voltage level that corresponds to a selected logic standard. Additionally, output driver **102** has three control lines which receive signals ENABLE, SB0 (Select Bit 0), and SB1 (Select Bit 1).

Input driver **104**, which has an input terminal to receive signals from I/O pad **106** and output buffer **102**, provides input signals to the PLD at the appropriate level of voltage, regardless of the voltage level of the signal receive on the input terminal. In addition, input driver **104** also receives control signal SB1 from programmable element **108**. Programmable elements **108** and **110** may be of any variety of memory cells. For example, elements **108** and **110** may be SRAM (static random access memory), EPROM (erasable programmable read-only memory), EEPROM (electrically erasable programmable read-only memory), or antifuses.

For convenience, simplicity and to reduce chip area, it is preferable that elements **108** and **110** be formed from the same variety of programmable elements as the PLD to which they are attached. Thus, if the PLD utilizes EEPROM elements (such as in the MAX **7000** family of PLDs available from Altera Corporation, San Jose, Calif.), each I/O circuit **100** should also include EEPROM elements for programmable elements **108** and **110**. Further, while such a configuration is preferable, it is not a requirement of the present invention (i.e., a PLD utilizing EEPROMs may be configured with I/O circuits **100** utilizing SRAM elements).

The operation of I/O circuit **100** depends on the status of programmable elements **108** and **110**. For a given set of programmable bits (i.e., setting the status of elements **108** and **110**), output driver **102** and input driver **104** are configured to convert PLD voltage levels to voltage levels corresponding to the selected logic standard. Further, output driver **102** does not change its output voltage levels until an ENABLE signal is received on the appropriate control line, as described more fully below. In contrast to output driver **102**, input driver **104** adjusts the voltage levels it operates with as soon as signal SB1 changes.

In the configuration shown in FIG. 1, where only two control bits are used (i.e., SB0 and SB1), there are four different sets of voltage levels which may be selected. Each voltage level corresponds to one or more of the appropriate voltages necessary to drive devices in accordance with a given logic standard.

For example, one possible I/O configuration for a given set of possible values of programmable elements **108** and **110** is given in the following Table 1:

TABLE 1

SB1	SB0	Logic Standard Voltages
0	0	TTL/CMOS
0	1	Open Drain
1	0	GTL/HSTL (non-terminated)
1	1	GTL/HSTL (terminated)

Thus, for example, if signals SB1 and SB0 are both set provide a logic low, output driver **102** and input driver **104** are configured to operate with TTL/CMOS voltage levels in interfacing with I/O pad **106**.

FIG. 2 shows a schematic circuit diagram of one embodiment of output driver **102** of FIG. 1. Output driver **102** includes inverter **202**, which is adapted to receive the ENABLE signal and NOR gate **204**, which receives the inverted ENABLE signal from inverter **202** and signal SB0 from element **110** (of FIG. 1). The output of NOR gate **204** is provided as one input to NAND gate **206**, while the OUT signal is provided as the other input. Additionally, the OUT signal is inverted by inverter **208** and provided as one input to NAND gate **210**, while the ENABLE signal is the other input signal.

The output of NAND gate **206** is provided to inverter **212**, while the output of NAND gate **210** is provided to inverter **214**. Inverters **212** and **214** are preferably both CMOS inverters which are formed by fabricating an n-channel MOSFET and a p-channel MOSFET with merged floating regions, as is well known in the art. Thus, inverters **212** and **214** are formed by n-channel MOSFETs **216** and **218**, respectively, and p-channel MOSFETs **220** and **222**, respectively. The outputs of inverters **212** and **214** are coupled to n-channel MOSFETs **224** and **226**, respectively.

Signal SB1 is provided to inverter **228**, whose output is coupled to transmission gate **230**. Signal SB1 is also coupled to the gate of n-channel MOSFET **232**. The input of transmission gate **230** is coupled to the output of NAND gate **210**, while the output of gate **230** is coupled to the gate of n-channel MOSFET **234**. MOSFET **234** is used to adjust the trip point of inverter **214**. The output of NAND gate **210** is also coupled to the gate of n-channel MOSFET **236**.

Inverter **214** provides an input signal to inverter **238** that is inverted and supplied as one input to NOR gate **240**. The other input for NOR gate **240** is the inverted SB1 signal output from inverter **228**. NOR gate **240** drives the gate of n-channel MOSFET **242**, which has its drain and source regions connected between MOSFET **236** and the output terminal of output driver **102** (designated as V_{OUT}).

Output driver **102**, which is active high (as described below), operates as follows. When ENABLE is low, the output of inverter **202** is high so that NOR gate **204** provides a low signal. The low signal is input to NAND gate **206**, which produces a high signal to inverter **212**. Inverter **212** inverts the high signal to drive the gate of n-channel MOSFET **224** with a low signal, which keeps MOSFET **224** turned off. At the same time, the low ENABLE signal is also provided as an input to NAND gate **210**, which produces a high signal to inverter **214**.

Inverter **214** inverts the high signal to drive the gate of n-channel MOSFET **226** with a low signal, which keeps MOSFET **226** turned off. Because both MOSFETs **224** and **226** are turned off, irrespective of signals SB1 and SB0, signal OUT is not passed to V_{OUT}. Thus, when ENABLE is low, output driver **102** is inactive.

Output driver **102** is turned on when ENABLE is set high. The logic standard applied by output driver **102** is deter-

mined by the status of Select Bits SB1 and SB0. The high ENABLE signal is input to inverter 202 and NAND gate 210, which potentially activates NOR gate 204 and NAND gate 210. The other input to NOR gate 204 is signal SB0, such that NOR gate 204 produces a high output if signal SB0 is low.

If the output of NOR gate 204 is low, then the output of NAND gate 206 is high, regardless of the state of signal OUT. A high output signal from NAND gate 206 is inverted to a low signal by inverter 212, the low signal preventing MOSFET 224 from turning on. MOSFET 224 has its drain and source nodes connected between predetermined voltage source V_{CCIO} and terminal V_{OUT}, respectively.

A high output signal from NOR gate 204 (i.e., when signal SB0 is low) is combined with signal OUT such that NAND gate 206 acts as an inverter on the OUT signal. The signal inverted by NAND gate 206, is inverted by inverter 212 such that the signal input to the gate of MOSFET 224 is the same as that of signal OUT. Thus, if signal OUT is high, MOSFET 224 is turned on and if signal OUT is low, MOSFET 224 is turned off.

The second MOSFET which controls the output signal is MOSFET 226, which is connected between predetermined voltage source V_{SSIO} and terminal V_{OUT} (while it is preferable that V_{SSIO} is separate from internal ground source V_{SS}—to reduce noise—the principles of the present invention may be practiced using a common ground). The state of MOSFET 226 is determined based upon signals SB1 and OUT. Signal OUT is inverted by inverter 208 and input to NAND gate 210, which together act as a buffer to signal OUT (that is controlled by signal ENABLE). Thus, signal OUT is provided as an input to inverter 214. The inverted signal controls MOSFET 226 such that MOSFET 226 is on when signal OUT is low, and off when signal OUT is high.

Signal SB1, which is inverted by inverter 228, drives the gate of MOSFET 232. The inverted SB1 signal determines whether transmission gate 230 passes the signal at its input (which corresponds to signal OUT). When transmission gate 230 is on, it passes signal OUT to the gate of MOSFET 234. The inverted SB1 signal is also provided as one input to NOR gate 240. The other input to NOR gate 240 is signal OUT (i.e., signal OUT, after it has been inverted twice by inverters 214 and 238). The output of NOR gate 240 drives the gate of MOSFET 242, which has a source region connected to terminal V_{OUT}. Signal OUT also drives the gate of MOSFET 236, such that MOSFET 236 is on when signal OUT is high.

The circuitry including inverters 228 and 238, NOR gate 240, transmission gate 230, and MOSFETs 232, 234, 236, and 242 provide noise reduction for output driver 102 during transitions of signal OUT from low to high when Select Signal SB1 is high (because when SB1 is low, NOR gate 240 always provides a low output keeping MOSFET 242 turned off—i.e., TTL and open drain).

While OUT is low, MOSFET 242 is on and MOSFET 236 is off. When OUT goes high, MOSFET 236 is immediately turned on such that MOSFETs 236 and 242 are on causing the gate and drain of MOSFET 226 to be tied together. Once the time delay introduced by inverter 236 and NOR gate 240 lapses, MOSFET 242 turns off and normal operation continues. Thus, noise is reduced during the low-to-high transition by temporarily coupling the gate and drain of MOSFET 226 together. Further, the noise reduction is only applicable during GTL/HSTL operations (i.e., when signal SB1 is high).

FIG. 3 shows one embodiment of input driver 104 as input driver circuit 300. Driver circuit 300 merges the TTL portion with the GTL portion to reduce transistor count and layout area. However, due to the merged circuitry, the TTL and GTL circuits may not be independently optimized. Driver circuit 300 includes p-channel MOSFETs 302 and 304, and n-channel MOSFET 306, all having a gate coupled to receive signal V_{OUT} from output driver 102 or I/O pad 106. MOSFET 302 is coupled between predetermined voltage source V_{CC} and one side of the source/drain channel of MOSFET 304. An additional p-channel MOSFET 308 is also coupled the source/drain channel of MOSFET 304.

The other side of the source/drain channel of MOSFET 304 is coupled to a series of inverters 314, 316, and 318, which provide signal IN to the PLD. N-channel MOSFET 320 has a source/drain channel coupled between the input of inverter 314 and MOSFET 306. The gate of MOSFET 320 is driven by inverted signal SB1 (which is inverted by inverter 322).

N-channel MOSFET 324 has a source/drain channel coupled between MOSFET 304 and ground, while n-channel MOSFET 326 is coupled between MOSFET 308 and ground, however, MOSFET 326 is diode-connected. The gates of MOSFETs 324 and 326 are coupled together and to one end of the source/drain channel of n-channel MOSFET 328, while the other end is coupled to ground. MOSFET 328 is driven by the inverted SB1 signal received from inverter 322.

P-channel MOSFET 310 and n-channel MOSFET 312 have their gates coupled together such that one of MOSFETs 310 and 312 is on at all times. The gates of MOSFETs 310 and 312 are coupled to receive signal SB1, which is the only Signal Bit utilized by input driver circuit 300. MOSFETs 310 and 312 also have their source/drain channels coupled together and to the gate of MOSFET 308 such that the gate of MOSFET 308 is always provided with one of predetermined voltages V_{CC} or V_{REF} (V_{REF} may typically be about 0.8 volts).

MOSFETs 302, 304, 308, 324 and 326 are coupled together to form a differential amplifier. The inputs to the differential amplifier are the gates of MOSFETs 304 and 308. MOSFET 304 receives the input signal from either output buffer 102 or I/O pad 106, while MOSFET 308 receives the predetermined reference voltage. The input signal is only compared to the reference voltage by the differential amplifier when the amplifier is activated by Select Signal SB1.

When signal SB1 is high—i.e., logic standard GTL or HSTL is selected—inverter 322 provides a low signal to the gates of MOSFETs 320 and 328, turning them both off. At the same time, the high SB1 signal is provided to the gates of MOSFETs 310 and 312, which turns MOSFET 310 off (because it is a p-channel device) and MOSFET 312 on (because it is an n-channel device). MOSFET 312 provides V_{REF} (which is a reference voltage, typically about 0.8 volts) to MOSFET 308, turning it on.

MOSFETs 324 and 326 are coupled together to produce a current mirror within the differential amplifier such that the current passing through MOSFETs 304 and 324 is substantially equal to the current passing through MOSFETs 308 and 326. The current mirror is turned on and off by MOSFET 328 in conjunction with signal SB1 (i.e, when SB1 is low, MOSFET 328 is turned on which grounds the gates of MOSFETs 324 and 326, effectively turning off the current mirror). Additionally, because MOSFET 320 is off when the current mirror is on (it is controlled by the same signal that controls MOSFET 328), the signal IN is directly related to the current passing through the branches of the current mirror.

However, if signal V_{OUT} is higher than V_{REF} when SB1 is high, the current mirror is not turned on because p-channel MOSFET 302 is off (such that the current from voltage source V_{CC} does not pass into the current mirror). Because the current mirror is off, the input to inverter 314 is low. The low signal is inverted three times and supplied as a high signal to terminal IN. Three inverters are provided to enable the driver circuit to drive circuits having increased loads by sizing inverter 314 to be smaller than inverters 316 and 318. Thus, inverters 316 and 318 act to buffer and amplify the signal output from inverter 314. The smaller size of inverter 314 is used to reduce the loading at the output of the input buffer to allow it to switch faster.

On the other hand, when signal V_{OUT} is lower than V_{REF} and SB1 is high, MOSFET 302 is on which turns on the current mirror. A current then passes down each branch of the current mirror and provides a high input to inverter 314. The high signal is inverted three times to provide a low signal to terminal IN.

A low SB1 signal turns on MOSFET 310 which provides V_{CC} to MOSFET 308, turning it off. The low SB1 signal also turns on MOSFET 328 which grounds the current mirror, and turns on MOSFET 320. MOSFET 320 acts in conjunction with MOSFET 306 to provide a current path depending on the state of signal V_{OUT} When signal VOUT is high, MOSFETs 306 and 320 are on which grounds the input to inverter 314. The grounded signal is inverted three times to provide a high signal to terminal IN. When signal V_{OUT} is low, MOSFETs 302 and 304 are turned on and MOSFET 306 is turned off. Thus, a high signal is input to inverter 314 which is inverted three times and provided as a low signal to terminal IN.

Operation of I/O circuit 100 may require additional settings by a user to properly program the buffer circuitry. For example, for use with the TTL/CMOS standards, V_{CCIO} is typically set about 5.0 volts, which provides a high signal from about 2.4 volts to about 3.5 volts. For open drain logic, I/O pad 106 is coupled to a terminating resistor, which sets the appropriate voltage levels because MOSFET 224 is permanently off (due to signal SB0 being set high).

GTL/HSTL non-terminated logic operates in a manner similar to open drain, in that MOSFET 224 is always off. However, the input voltage levels are set by the value of the reference voltage V_{REF} . For GTL/HSTL terminated, the voltage levels are determined by setting V_{CCIO} to be equal to the termination voltage (typically from about 1.2 volts to about 1.6 volts).

FIG. 4 shows an alternate embodiment of input buffer ~~102~~ 104 as buffer circuit 400. In buffer 400, the TTL and GTL input driving circuits are not merged, requiring higher transistor count than buffer 300. However, buffer 400 provides the capability to independently optimize the operational speed of the TTL and GTL input buffers.

Buffer circuit 400 includes inverter 402 and n-channel MOSFET 404 which are adapted to receive signal V_{OUT} from output buffer 102 or I/O pad 106. MOSFET 404, which has a source connected to drive the gate of p-channel MOSFET 406, is itself driven by Select Signal SB1 (once again, the only Select Signal utilized by input buffer 104). Select Signal SB1 is also inverted by inverter 408 and provided to n-channel MOSFETs 410 and 412. MOSFET 410 connects the inverted V_{OUT} signal (from inverter 402) to the input of inverter 414, which is coupled in series through inverters 416 and 418 to terminal IN.

P-channel MOSFET 420 is coupled to act as the current source for the current mirror formed by n-channel MOSFETs 422 and 424, with MOSFET 422 being diode-connected. P-channel MOSFET 426 is coupled to mirror the characteristics of MOSFET 406, but is constantly driven on by reference voltage V_{REF}. Thus, the two branches of the current mirror are formed by MOSFET pairs 422/426 and 406/424.

Similarly to MOSFET 328 of FIG. 3, n-channel MOSFET 412 turns the current mirror on and off in conjunction with signal SB1 by grounding the gates of MOSFETs 422 and 424. Additionally, p-channel MOSFET 428, which is connected between reference voltage V_{CC} and the gate of MOSFETs 406 and 420, keeps the current mirror turned off when SB1 is low by providing V_{CC} to the gates of MOSFETs 406 and 420 to turn them off.

Buffer circuit 400 operates as follows. When signal SB1 is low, the current mirror is turned off and MOSFET 410 is turned on. Therefore, the V_{OUT} signal applied by output buffer 102 or I/O pad 106 is level translated first by inverter 402 then inverted three times (by inverters 414, 416, and 418) back to its original state and provided to terminal IN (i.e., a high signal V_{OUT} ends up as a high signal at terminal IN and vice versa).

When signal SB1 is high, MOSFETS 410, 412, and 428 are turned off, which terminates the direct path from terminal V_{OUT} to terminal IN and turns on the current mirror. MOSFET 404, which is coupled to terminal V_{OUT}, is turned on to provide signal V_{OUT} as a driving signal to the gate of MOSFET 406. The output of the current mirror is taken from a node between MOSFETS 406 and 424 and is coupled to the input of inverter 414.

If signal V_{OUT} is lower than V_{REF}, MOSFETS 406 and 420 are turned on, activating the current mirror to cause a high signal to be input to inverter 414. The high signal is inverted three times to provide a low signal to terminal IN. If signal V_{OUT} is higher than V_{REF}, MOSFETS 406 and 420 are turned off, de-activating the current mirror to cause a low signal to be input to inverter 414. The low signal is inverted three times to provide a high signal to terminal IN.

FIG. 5 shows another alternate embodiment of input buffer ~~402~~ 104 as buffer circuit 500. Buffer circuit 500 is substantially similar to buffer circuit 400 of FIG. 4, except for a slight rearrangement of input signals which enables two inverters to be eliminated. The elimination of the inverters provides a buffer circuit requiring slightly less chip area than buffer 400. However, because of the eliminated inversion stage, buffer circuit 500 may only be used to drive smaller loads than buffer circuit 400. Circuit components that are the same in buffer circuits 400 and 500 are numbered using buffer circuit 400's reference numerals. Accordingly, the discussion above for those components applies likewise to buffer circuit 500 unless otherwise described.

The differences between buffer circuits 400 and 500 are as follows. Buffer 500 is implemented without inverters 402 and 418. Thus, when the current mirror is inactive, the signal from terminal V_{OUT} is only inverted twice, instead of four times, before being received by terminal IN. Additionally, because there are only two inverters in series between the current mirror and terminal IN, the current mirror must be configured to provide output signals which are inverted from the output signals of the current mirror of FIG. 4.

Whereas signal V_{OUT} is supplied as an input to MOSFET 404 in buffer 400, signal V_{OUT} is provided as an input to MOSFET 426 in buffer 500 (i.e., the opposing branch of the current mirror). Additionally, reference voltage V_{REF}, which constantly drives MOSFET 426 on in buffer 400, is instead provided as the input to MOSFET 404 in buffer 500. The